IARJSET

ISSN (Online) 2393-8021
ISSN (Print) 2394-1588

International Advanced Research Journal in Science, Engineering and Technology

ISO 3297:2007 Certified

Vol. 3, Issue 7, July 2016

Designing Parity Preserving P2r Gate Reversible Circuit

S. Suma[1], D. Mahesh Kumar[2]

M.Tech, PG Student[1]

Associate Professor[2]

Abstract: In current scenario, the reversible logic design attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, Toffoli gate etc. This paper present a basic reversible gate to build more complicated circuits which can be implemented in ALU, some sequential circuits as well as in some combinational circuits. It also gives brief idea to build adder circuits using the basic reversible gate like peres gate This paper proposes a novel 4x4 bit reversible fault tolerant multiplier circuit which can multiply two 4-bit numbers. This based on two concepts. The partial products can be generated in parallel using PG gates and thereafter the addition is done by using reversible parallel adder designed from PFAG gates. Thus, this paper provides idea for building of more complex system which can execute more complicated operations using reversible logic.

Keywords: Garbage output, Peres gate, PFAG, Reversible logic

I. INTRODUCTION

Energy dissipation is an important consideration in VLSI design. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation. This principle is further supported by Bennett that zero energy dissipation can be achieved only when the circuit contains reversible gates [2].Information is lost when the input vector cannot be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [1,2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Reversible circuits are also interesting because the loss of bits of information implies energy loss. However, reversible logic is suffering from two problems. Firstly, there is a lack of technologies with which to build reversible gates.

Work is certainly continuing in this area. Secondly, while there is much research into how to design combinational circuits using reversible logic, there is little in the area of sequential reversible logic implementations. . "To establish the relevance of reversible and quantum computing it seems appropriate to note that the VLSI industry is moving at high speed towards miniaturization. With miniaturization it faces two issues: i) A considerable amount of energy gets dissipated in VLSI circuits and ii) the size of the transistors are approaching the quantum limits where tunneling and other quantum phenomena are likely to appear. Thus, we need a superior technology that can circumvent these problems. Power dissipation is one of the important parameters in the digital circuit design. In VLSI circuit designing where power dissipation plays an important role, there has been an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking them with higher frequencies. The logic elements are normally irreversible in nature and according to Landauer's principle irreversible logic computation results in energy dissipation due to power loss. This is because; erasure of each bit of information dissipates at least KTln2 Joules of energy where K is Bolt zamann's constant and T is the absolute temperature at which the operation is performed. By 2020 this will become a substantial part of energy dissipation, if Moore's law continues to be in effect which states that processing power will double every 18 months. This particular problem of VLSI designing was realized by Feynman and Ben net in 1970s. In 1973 Ben net [2] had shown that energy dissipation problem of VLSI circuits can be circumvented by using reversible logic. This is so because reversible computation does not require erasing any bit of information and consequently it does not dissipate any energy for computation. .

In a short period the reversible computation has emerged as a promising technology having applications in low power CMOS, nanotechnology, optical computing ,optical information processing, DNA computing, bioinformatics, digital signal processing and quantum computing. It is very clear that reversible circuits will play dominant role in future technologies. These facts motivated many researchers to work in this domain A reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a unique output pattern. Thus, Reversible logic circuits avoid energy loss by un computing the computed information by recycling the

IARJSET
ISSN (Online) 2393-8021
ISSN (Print) 2394-1588
International Advanced Research Journal in Science, Engineering and Technology
ISO 3297:2007 Certified
Vol. 3, Issue 7, July 2016

energy in the system. In the design of reversible circuits two restrictions should be considered; firstly, Fan-out is not permitted and secondly, Feedback from gate outputs to inputs is not permitted. Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa . So, there is a one-to-one mapping between input and output vector. A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation.

Reduction of these parameters is the main design focus. Reversible circuits for different purposes like half adder, full adder multiplier[3-11,15] have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral components of every computer system, cellular phone and most digital audio/video devices.

II. REVERSIBILITY AND BASIC EVERSIBLE GATES

The gate/circuit that does not loose information is called reversible. A Reversible circuit has the facility to generate a unique output vector from each input vector, and vice versa.

III. REVERSIBLE GATES

Different reversible gates include Fredkin gate, Peres gate, IG gate etc. are shown below

1. Feynman Gate: Feynman gate is a universal gate which is used for signal copying purposes or toobtain the complement of the input signal. The block diagram of Feynman gate is shown in fig.1:

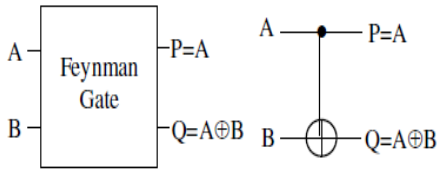

Fig. 1: Feynman Gate

2. Fredkin Gate: It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2:

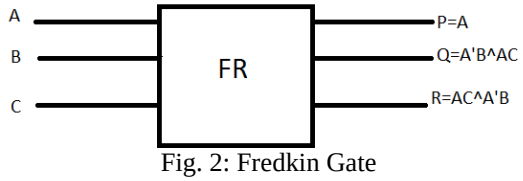

Fig. 2: Fredkin Gate

3. Peres Gate: It is a basic reversible gate which has Inputs and 3-outputs having inputs (A, B, C) and the Mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3:

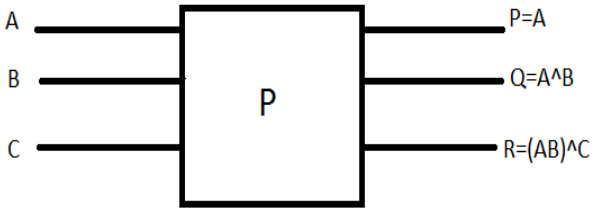

Fig. 3: Peres Gate

4. Toffoli Gate: Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4:

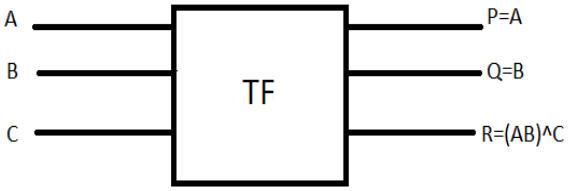

Fig. 4: Toffoli Gate

5. TSG Gate: TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5:

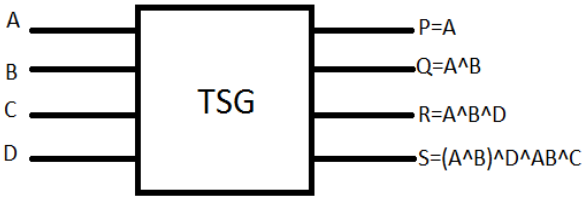

Fig. 5: TSG Gate

IV. REVERSIBLE 4- BIT FULL ADDER

The gate used in implementing a reversible ripple-carry full adder is the TSG gate [4]. The TSG gate functions like a full adder. A reversible ripple-carry adder is faster than the non-reversible adder, since the computation of carry in a reversible adder does not require the computation of previous stage carry (as indicated in the critical paths).

When previous stage carry is being forwarded in the reversible adder, the computation of previous stage carry and computation regarding sum is done simultaneously whereas in an irreversible adder the next stage carry cannot start any computation till previous stage carry is fully generated. The critical paths of 4bit reversible and irreversible ripple-carry adders are as shown in fig.6 and fig.7

IARJSET
ISSN (Online) 2393-8021
ISSN (Print) 2394-1588
International Advanced Research Journal in Science, Engineering and Technology
ISO 3297:2007 Certified
Vol. 3, Issue 7, July 2016

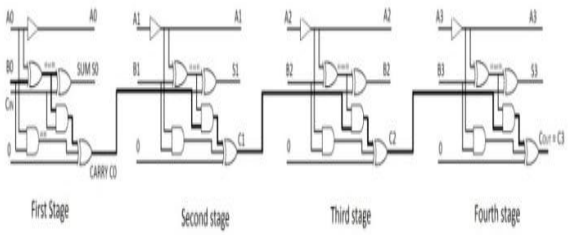

Fig. 6: Critical Path of 4-bit reversible adder

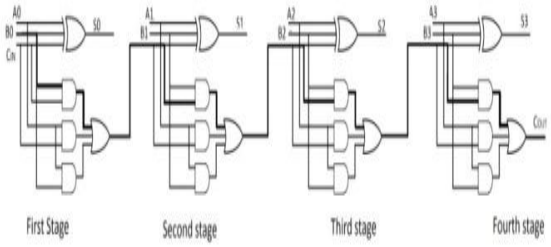

Fig. 7: Critical Path of 4 bit irreversible adder.

V. CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation In the proposed work , we designed a reversible multiplier using pg and pfag gate with reduced gate count and reduced garbage output. The comparison table shows clear idea of the system with the existing one. Reduction in number of gate can reduce the circuit complexity . The chance for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

REFERENCES

[1] R. Landuer, IBM, Irreversibility and heat generation in the computing process, J. Res. Develop., 5 (1961) 183.
[2] C. H. Bennet, Logical reversibility of computation, IBM J. Res. Dev., 6 (1973) 525
[3] V. V. Shende, I.L. Markov, and S.S. Bullock, Synthesis of quantum logic circuits, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., 25 (2006) 1000
[4] M. Haghparast, S. J. Jassbi, K. Navi and O. Hashemipour, "Design of a novel reversible multiplier circuit using HNG gate in nanotechnology", World Appl. Sci. 1., 3 (2008) 974.
[5] R. Landuer, IBM, Irreversibility and heat generation in the computing process, J. Res. Develop., 5 (1961) 183.
[6] C. H. Bennet, Logical reversibility of computation, IBM J. Res. Dev., 6 (1973) 525
[7] V. V. Shende, I.L. Markov, and S.S. Bullock, Synthesis of quantum logic circuits, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., 25 (2006) 1000
[8] M. Haghparast, S. J. Jassbi, K. Navi and O. Hashemipour, "Design of a novel reversible multiplier circuit using HNG gate in nanotechnology", World Appl. Sci. 1., 3 (2008) 974.
[9] M. Haghparast and K. Navi, "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems". J. Applied Sci., 7 (2007) 3995.
[10] T. Toffoli, “Reversible computing”, In Automata, Languages and Programming, Springer-Verlag, pp. 632-644, 1980.
[11] H.P.Sinha ,Nidhi sayal” Design of fault tolerant reversible multiplier” ijsee .1(2012)
[12] P. Kerntopf, A new heuristic algorithm for reversible logic synthesis, In Proceedings of the IEEE Design Automation Conference (2004) 834.
[13] E. Fredkin and T Toffoli, "Conservative logic," Int. 1. Theor. Phys., vol. 21, no. 3-4, pp. 219-253, 1982.
[14] H. Thaplyal and M. B. Srinivas, "Novel reversible multiplier architecture using reversible TSG gate", IEEE Int. Conf Computer Systems and Applications (2006) 100.